OIPE JC177
MAR 17 2004
PATENT & TRADEMARK OFFICE

FIG. 1
PRIOR ART

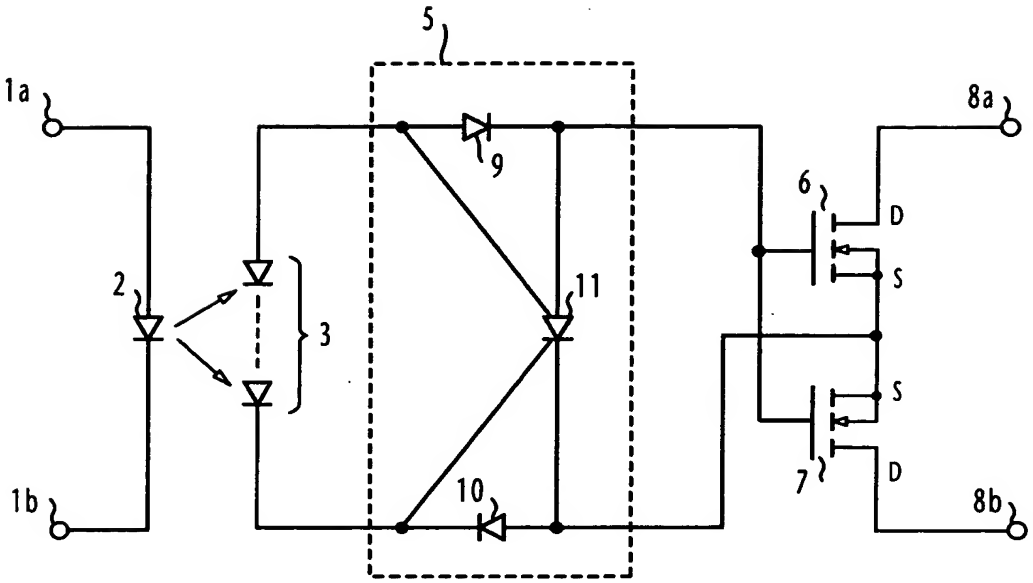


FIG. 2
PRIOR ART

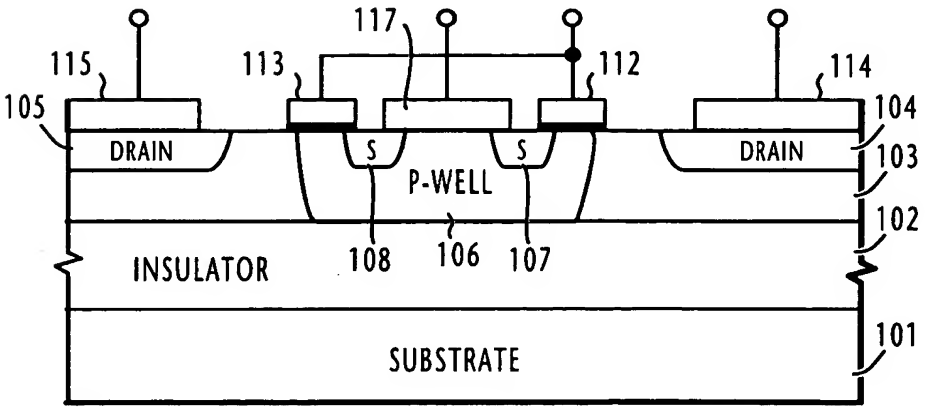


FIG. 3

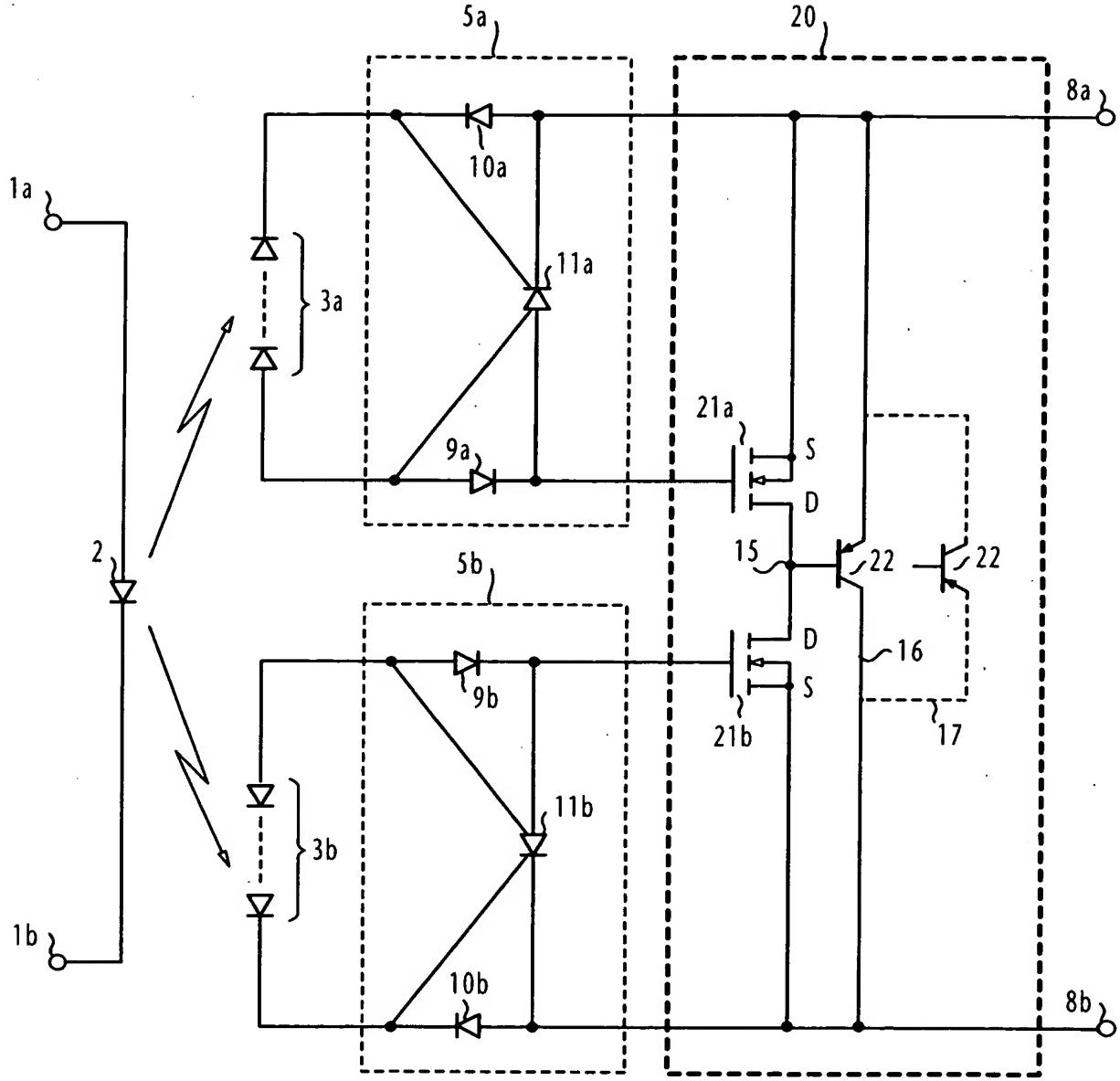

5a
20
8a
10a
1a
11a
3a
21a
S
9a
D
2
15
22
22
5b
D
16
9b
S
21b
17
11b
3b
1b
10b
8b

FIG. 4

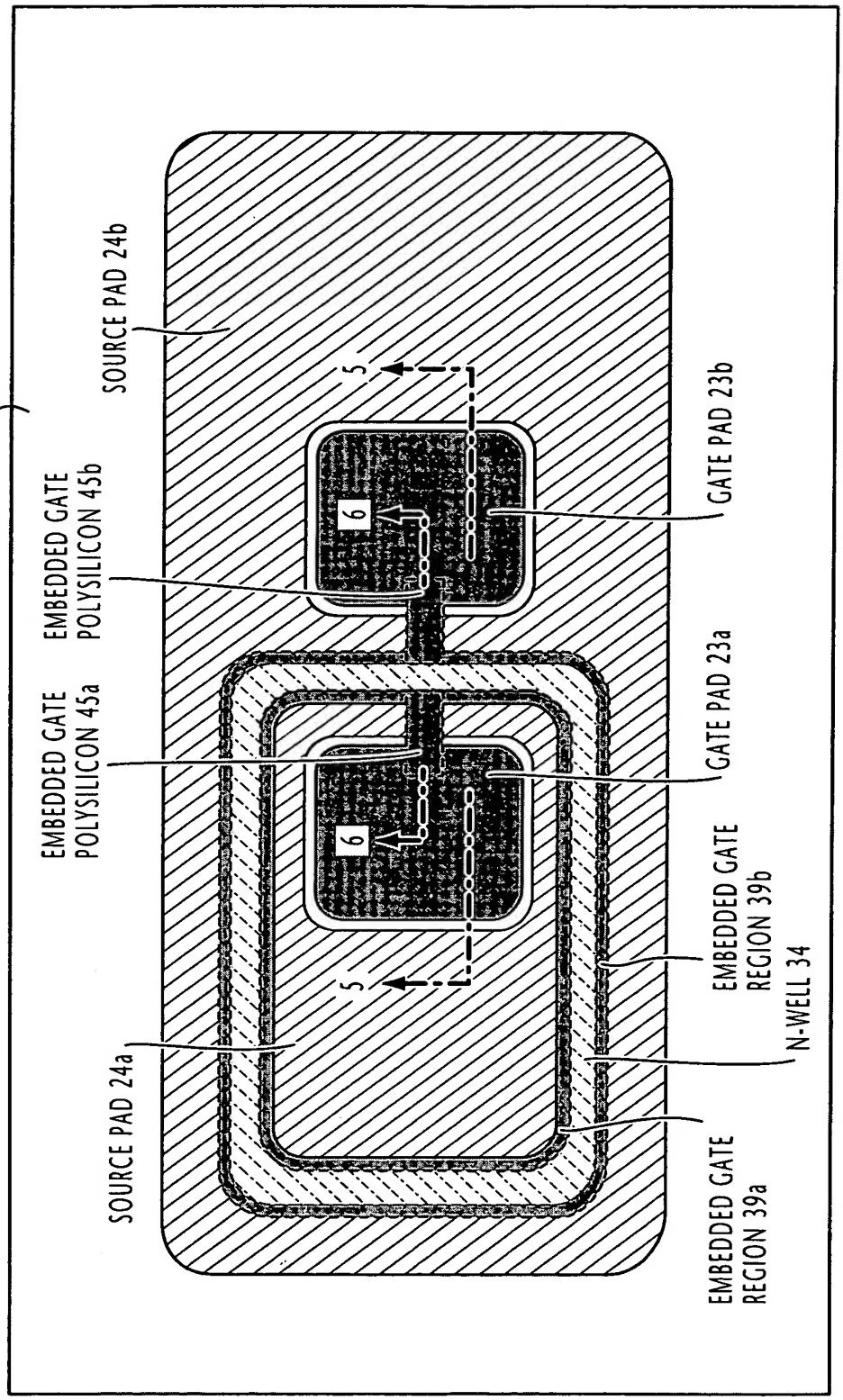

20
41
SOURCE PAD 24b
EMBEDDED GATE POLYSILICON 45b
EMBEDDED GATE POLYSILICON 45a
SOURCE PAD 24a
EMBEDDED GATE REGION 39a
EMBEDDED GATE REGION 39b
N-WELL 34
GATE PAD 23b
GATE PAD 23a
5
5
6
6

FIG. 5

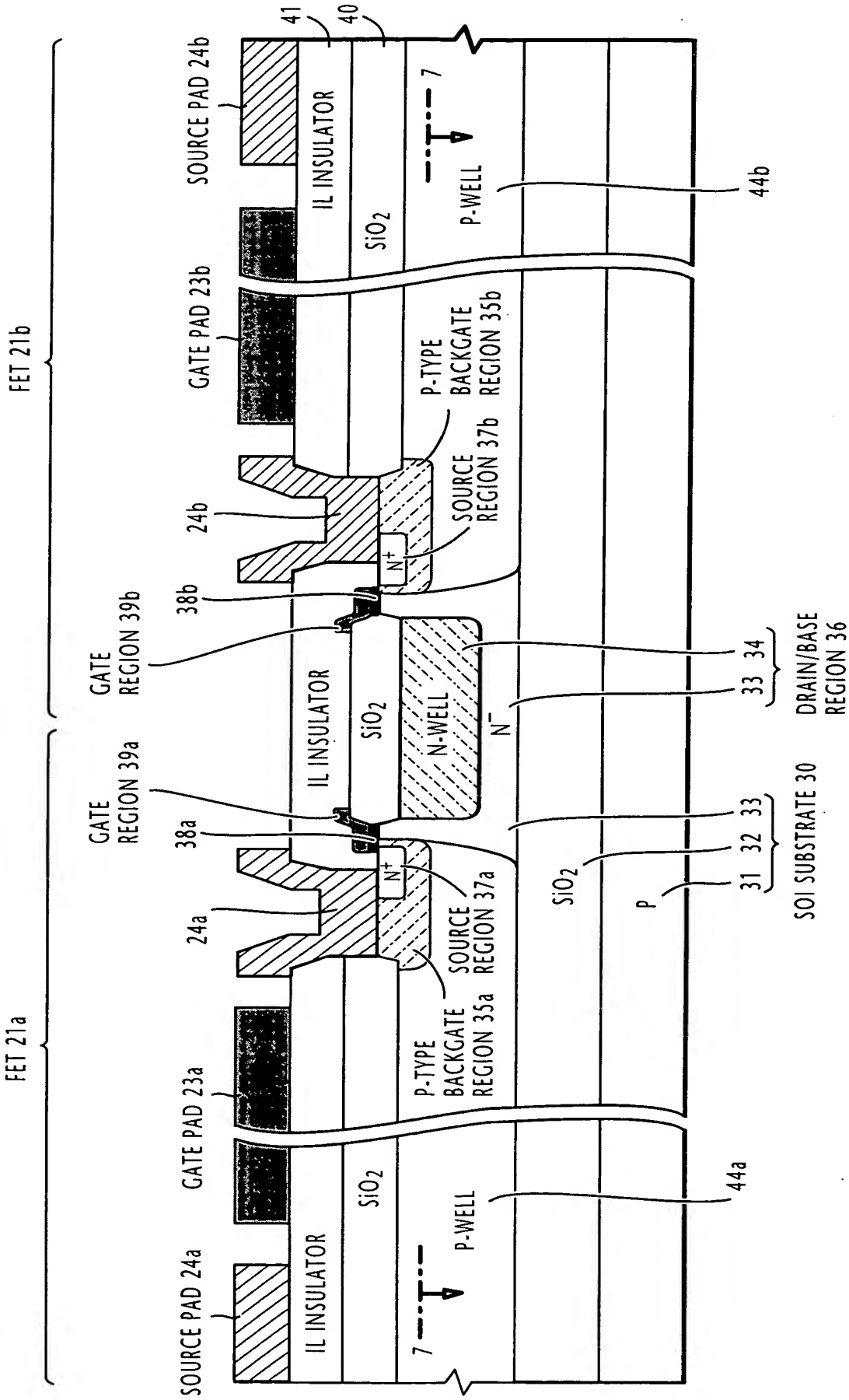

FET 21a
FET 21b
SOURCE PAD 24a
GATE PAD 23a
IL INSULATOR
SiO_2
P-WELL
7
44a
P-TYPE BACKGATE REGION 35a
SOURCE REGION 37a
N^+
24a
38a
GATE REGION 39a
SiO_2
P
31 32 33
SOI SUBSTRATE 30
N-WELL
N^-
33 34
DRAIN/BASE REGION 36
GATE REGION 39b
38b
24b
SOURCE REGION 37b
P-TYPE BACKGATE REGION 35b
GATE PAD 23b
SOURCE PAD 24b
41
40
44b

FIG. 6

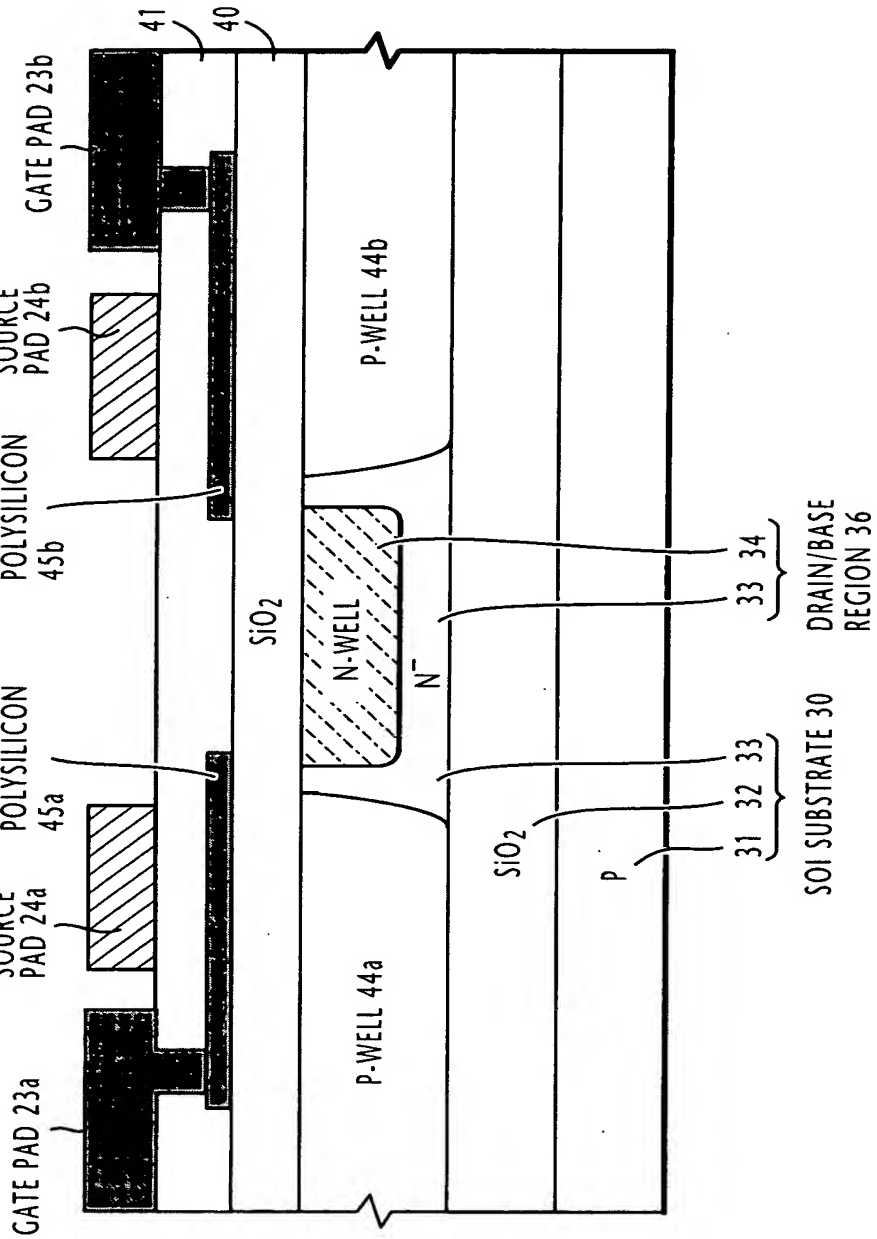

41
40
GATE PAD 23b
SOURCE PAD 24b
GATE POLYSILICON 45b
P-WELL 44b
SiO_2
N-WELL
N^-
33 34
DRAIN/BASE REGION 36
GATE POLYSILICON 45a
SOURCE PAD 24a
GATE PAD 23a
P-WELL 44a
SiO_2
P
31 32 33
SOI SUBSTRATE 30

FIG. 7

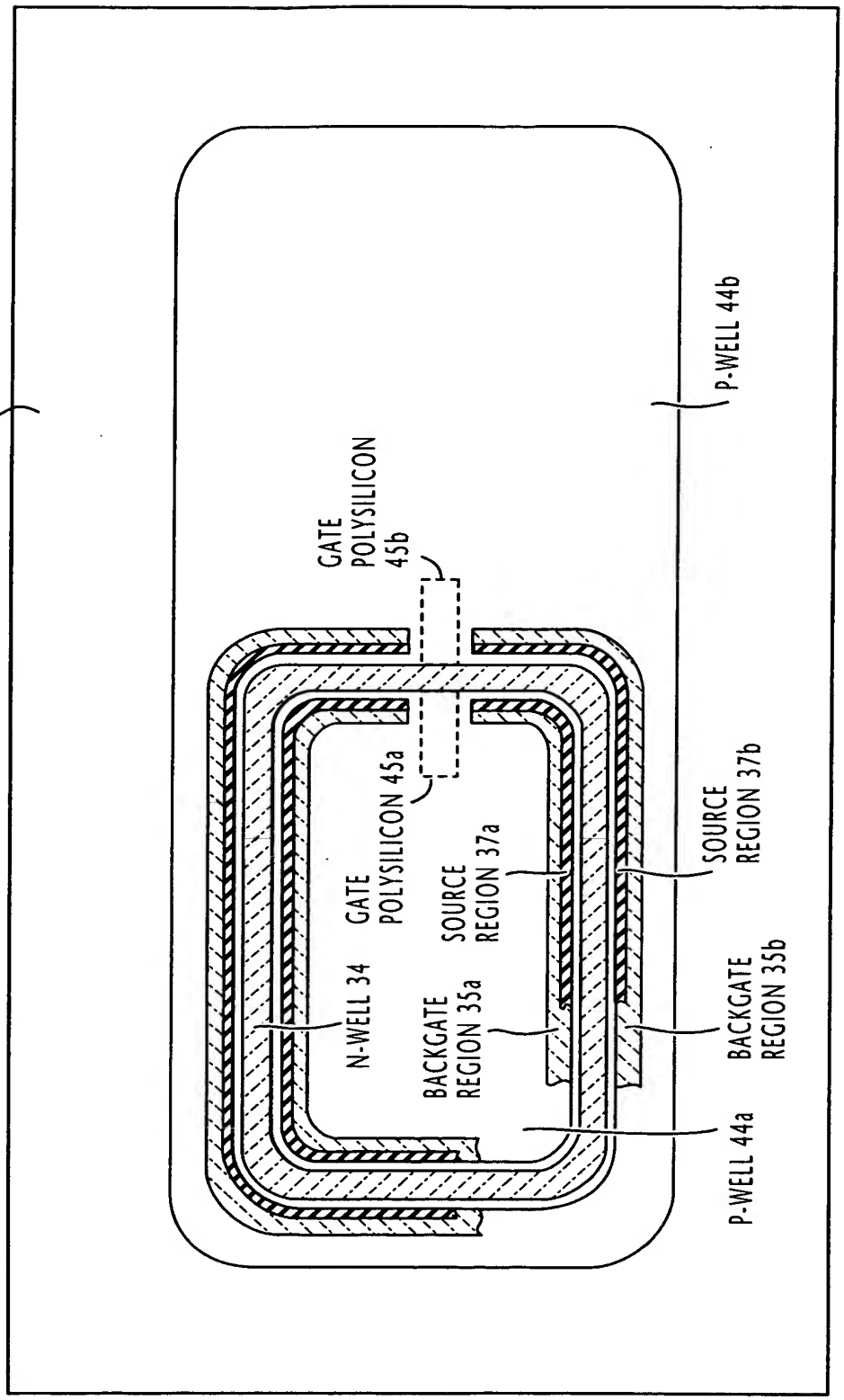

20
N- LAYER 33
P-WELL 44b
GATE POLYSILICON 45b
GATE POLYSILICON 45a
SOURCE REGION 37a
SOURCE REGION 37b
N-WELL 34
BACKGATE REGION 35a
BACKGATE REGION 35b
P-WELL 44a

FIG. 8

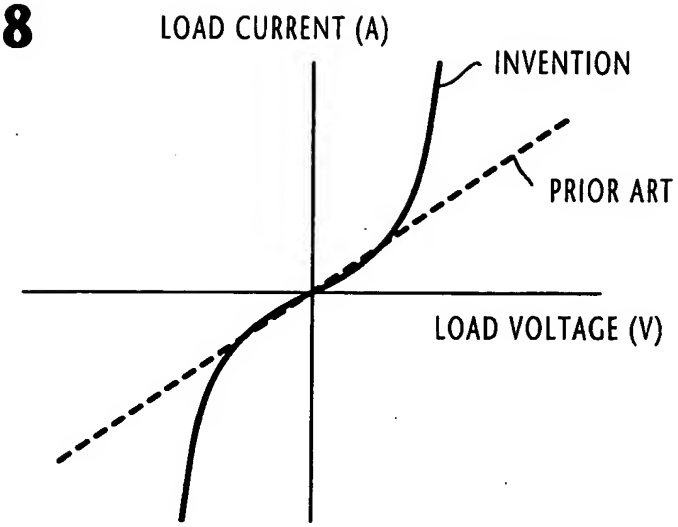
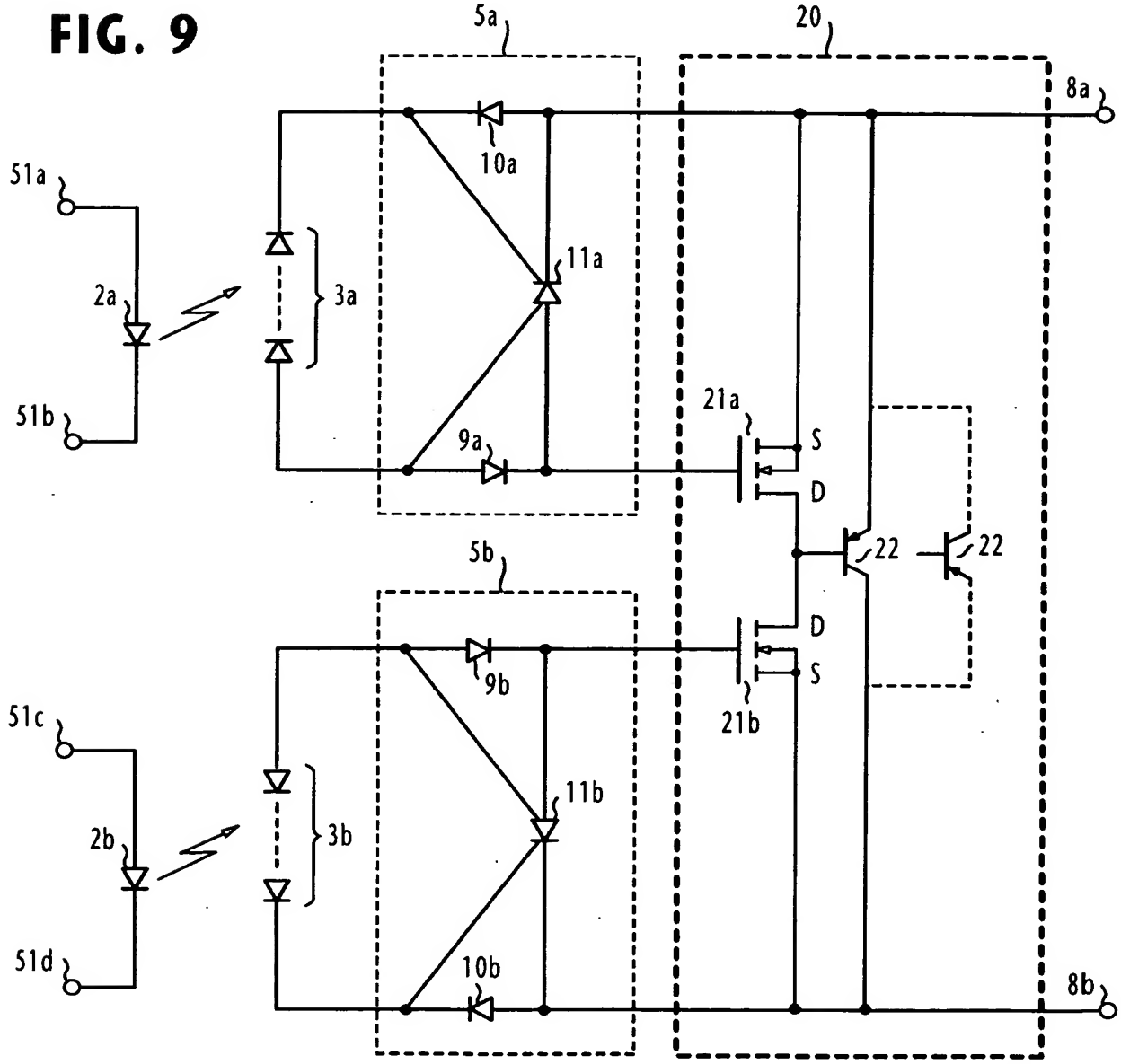

LOAD CURRENT (A)
INVENTION
PRIOR ART
LOAD VOLTAGE (V)

FIG. 9


5a
20
8a
51a
10a
11a
2a
3a
51b
21a
S
9a
D
22
22
5b
D
9b
S
51c
21b
11b
2b
3b
51d
10b
8b